IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

TELCORDIA TECHNOLOGIES, INC.,	)	
	)	
Plaintiff/Counterclaim Defendant,	)	
	)	
v.	)	C.A. No. 04-876-GMS
	)	
CISCO SYSTEMS, INC.,	)	
	)	
Defendant/Counterclaim Plaintiff.	)	
	)	

OPENING BRIEF IN SUPPORT OF DEFENDANT CISCO SYSTEMS, INC.'S MOTION FOR JUDGMENT AS A MATTER OF LAW

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I. NATURE AND STAGE OF THE PROCEEDING

Telcordia filed this patent infringement lawsuit against Cisco in July 2004, asserting U.S. Patent Nos. 4,893,306 ("the '306 patent"), RE 36,633 ("the '633 patent"), and 4,835,763 ("the '763 patent"). This Court held a jury trial on all issues from April 30 to May 10, 2007.[1] At the close of evidence, Cisco brought motions for judgment as a matter of law pursuant to Rule 50(a). D.I. 359 at 2005:23-2013:25. The Court reserved judgment on Cisco's motions. *Id.* at 2015:17-2016:13. The jury returned a verdict in favor of Telcordia on the liability issues, and the Court entered judgment of infringement in favor of Telcordia on the '763 and '633 patents on May 16, 2007. D.I. 348.

II. SUMMARY OF THE ARGUMENT

Pursuant to Rule 50, a court may render judgment as a matter of law after the moving party is fully heard on an issue at trial, if "there is no legally sufficient evidentiary basis for a reasonable jury to find for that party on that issue." *Walter v. Holiday Inns, Inc.*, 985 F.2d 1232, 1238 (3d Cir. 1993). To prevail on a renewed motion for judgment as a matter of law following a jury trial, a party "'must show that the jury's findings, presumed or express, are not supported by substantial evidence or, if they were, that the legal conclusion(s) implied [by] the jury's verdict cannot in law be supported by those findings.'" *Pannu v. Iolab Corp.*, 155 F.3d 1344, 1348 (Fed. Cir. 1998) (citations omitted).

Cisco hereby renews its motions for judgment as a matter of law on four issues: (1) non-infringement of the '763 patent; (2) invalidity of the '763 patent for failure to meet the definiteness requirement of 35 U.S.C. § 112, ¶2; (3) invalidity of the '633 patent as obvious, or

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[1] Because Telcordia did not oppose summary judgment of non-infringement of the '306 patent, infringement of that patent was not tried to the jury. The Court has issued an Order granting summary judgment of non-infringement on five grounds requested by Cisco. D.I. 341.

alternatively, for improper inventorship; and (4) invalidity of the '306 patent as anticipated or as obvious. Cisco requests that the Court enter judgment as a matter of law in its favor on these issues based on the weight of the evidence presented at trial and for the reasons set forth below.

III. STATEMENT OF FACTS

The pertinent facts are set forth in the Argument sections, as appropriate.

IV. CISCO IS ENTITLED TO JUDGMENT OF NON-INFRINGEMENT OF THE '763 PATENT AS A MATTER OF LAW

Judgment of non-infringement of the '763 patent as a matter of law is appropriate because the trial record establishes beyond question that the accused products do not insert error signals "following demultiplexing," as required by claims 1, 2, 7, and 8. As a matter of law, an accused device cannot infringe if even a single limitation is not satisfied. *Digital Biometrics, Inc. v. Identix, Inc.*, 149 F.3d 1335, 1349 (Fed. Cir. 1998).

During the claim construction proceedings, the central dispute for the '763 patent revolved around the insertion of error signals and whether insertion of those signals could occur in the claimed inventions before the high-level signal is demultiplexed. In view of the fact that Cisco's products insert errors signals before demultiplexing, Telcordia insisted during the claim construction proceedings that the claims of the '763 patent were broad enough to cover systems, including Cisco's products, that insert error signals before demultiplexing – despite the clear teaching of the '763 patent to the contrary.

The Court rejected Telcordia's position and held that the asserted claims require the error signals to be inserted "following demultiplexing." D.I. 179 at 2. Thus, to infringe the asserted claims, the accused products must insert error signals following demultiplexing in response to a high-level failure.

At trial, Cisco's expert, Dr. Wayne Grover, explained why the '763 patent requires the error signals to be inserted following demultiplexing:

> Q: Now, why in the '763 patent are the error signals put in after demultiplexing?
>
> A: That is a – it is not arbitrary. ***At the time, the technology we had for multiplexing and demultiplexing could only completely demultiplex the line signal to see any of the channels. It couldn't, for instance, have put error signals in beforehand.*** It needed to completely demultiplex the whole line signal. And then that's the only chance it has to access these signals to do something such as put an error signal in.
>
> So basically the technology at the time also is the reason you see in the patent that we are putting error signals in after demultiplexing. ***It is really the only way that we could have implemented this.***

D.I. 359 at 1779:2-15.[2] Telcordia's expert, Dr. Paul Prucnal, did not refute Dr. Grover's testimony that demultiplexing was required before inserting error signals at the time the '763 patent was filed due to the limitations of the technology described in the patent.

Dr. Grover also explained why Cisco's products do not require errors to be inserted following demultiplexing:

> Q: Is it still true today that the only way that you could put error signals on is first taking apart the six channels and breaking them into their individual channels?
>
> A: No. Things have changed. In fact, not surprisingly, nearly 20 years of advancements in technology . . . . ***One of the things that we can do now, Cisco products actually take advantage of this technical advance, they will manipulate the channels individually while in the multiplexed form*** to do many functions. And one of them is to put the error indication signals in.

D.I. 359 at 1779:16 – 1780:8. This testimony was also undisputed by Dr. Prucnal.

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[2] Emphases supplied throughout, unless otherwise noted.

The infringement theory Telcordia presented at trial was that the pointer processor in Cisco's products performs the required demultiplexing and inserts the required error signals following that demultiplexing. There is no support in the record for Telcordia's infringement theory as a matter of law, because there is no evidentiary basis from which a reasonable jury could find either (1) that the pointer processor performs the demultiplexing required by the claims, or (2) that the error signals inserted by the pointer processor are inserted in response to a high-level failure as required by the claims.

A. No Reasonable Jury Could Have Found That The Pointer Processor Performs The Demultiplexing Required By The '763 Patent

1. There Is No Dispute That The Demultiplexer Is The Cross-Connect

At trial, both experts agreed that the cross-connect in Cisco's products – not the pointer processor – is the claimed demultiplexer. Telcordia's expert, Dr. Prucnal, testified that, after "diligently" studying Cisco's products, he identified ***only*** the cross-connect as the demultiplexer:

> Q: And when you were asked to list what a demultiplexer is, you listed the cross connect circuitry. This is a complete representation of your portion on this part of the claim, isn't it?
>
> A: Yes, this is a demultiplexer.
>
> Q: All right. And for this portion of the claim ***where you are asked to list what a demultiplexer is, you didn't list a pointer processor or anything else, you just listed the cross connect circuitry.*** Isn't that fair?
>
> A: That's fair.

D.I. 354 at 1123:14-24; *id.* at 1126:24-1127:13 (cross-connect identified as the demultiplexer after "diligently" analyzing Cisco's products). Dr. Grover agreed that it is the cross-connect in Cisco's products that is the claimed demultiplexer. D.I. 359 at 1781:19-25.

Both experts also agreed that Cisco's products insert error signals before, not following, the claimed demultiplexer. Dr. Grover testified that error signals are inserted before, not after, the cross-connect. *Id.* at 1782:1-17. Dr. Prucnal agreed:

> Q: So the claim requires insertion of error signals. Right?
>
> A: Yes.
>
> Q: And it requires that those error signals be inserted after demultiplexing. Right?
>
> A: The Judge's claim construction does that, yes.
>
> Q: And this place where you have said the error signals are being inserted is in this larger box that we have labeled No. 2, the BTC chip. Right?
>
> A: Right.
>
> Q: And that is ***before, not after, the cross-connect.*** Isn't that fair?
>
> A: That's correct.

D.I. 354 at 1129:22 – 1130:9; *see also id.* at 1125:7-22.

Because Dr. Prucnal conceded, as he must, that it is the cross-connect, not the pointer processor, that is the claimed demultiplexer, Cisco's non-infringement becomes a purely legal matter. Where it is undisputed that a patent claim requires a demultiplexer and requires demultiplexing, can the demultiplexing claim requirement be satisfied by something other than the undisputed demultiplexer of the claim? Both law and logic dictate that the demultiplexing of the claim must be performed by the claimed demultiplexer. *See, e.g., Level One Communications, Inc. v. Seeq Tech., Inc.*, 987 F. Supp. 1191, 1206 (N.D. Cal. 1997) (holding that the claim term "'multiplexing' clearly corresponds to ***the*** multiplexer" in rejecting argument that the "multiplexing" step in a method claim was written in step-plus-function form).

It is well-established that a patentee cannot rely on unclaimed elements to satisfy the requirements of a claim when inclusion of those additional unclaimed elements would be at odds with the language of the claim. *See, e.g.*, *Spectrum Int'l v. Sterilite Corp.*, 164 F.3d 1372, 1377 (Fed. Cir. 1998);[3] *Ecolochem, Inc. v. Southern Cal. Edison Co.*, No. 95-1320, 1996 U.S. App. LEXIS 13330, at *8 (Fed. Cir. June 5, 1996) (attached as Exhibit 1) ("Placement of 'comprising' before recitation of steps, however, results in a 'comprising' claim that would cover a process that includes additional steps, not one that uses an additional unrecited element for accomplishing a claimed step."). Simply put, as a matter of law, Telcordia cannot rely on an unclaimed alleged second demultiplexer to satisfy the "following demultiplexing" requirement because reliance on an unclaimed demultiplexer instead of the claimed demultiplexer would be at odds with the logic and structure of the claims.

2. There Is No Dispute That Demultiplexing Is Not Complete Until After The Cross-Connect

There is a second, independent reason why no reasonable jury could have found that the pointer processor performs the demultiplexing required by the claims, and thus there is non-infringement as a matter of law. Because the cross-connect is indeed the demultiplexer in Cisco's products, Dr. Prucnal had to agree at trial that the required demultiplexing is not complete until *after* the cross-connect even if one were to accept that the pointer processor participates in demultiplexing:

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[3] In *Spectrum*, the asserted claims were directed to a crate, and required the bottom wall of the crate to merge with the bottom portion of the front wall. In the accused crates, the bottom wall merged with a flat layer of plastic – not with the bottom portion of the front wall, as claimed. The patentee argued that the accused products satisfied the claim requirements anyway because the flat layer of plastic in the accused products constituted *both* the top and bottom portions of a front wall, and the merger with the top portion was merely an unclaimed element. The Federal Circuit rejected the patentee's argument, noting that the term "'comprising' [cannot] alter the scope of the merger element in the claim at issue here" and "is not a weasel word with which to abrogate claim limitations." *Id.* at 1379-81

> Q: But completion of the [de]multiplexing, as you understand Cisco's products, doesn't happen until the cross-connect, where you get the dropping of the communications; correct?
>
> A: Yes, ***the final stage of the demultiplexing and its completion, as you said, is – is done at the cross-connect.***

D.I. 354 at 1128:15-21.

In its claim construction, the Court made clear that the claims require the insertion of error signals "following demultiplexing" of the high-level signal into its constituent channels. As a result, the demultiplexing must be complete before the error signals are inserted. *See, e.g.*, *Oak Tech., Inc. v. ITC*, 248 F.3d 1316, 1323-29 (Fed. Cir. 2001).[4] There is no dispute that the demultiplexing required by the claims is not complete until after the cross-connect, and that all error signals are inserted before the cross-connect.

3. No Reasonable Jury Could Have Found That The Pointer Processor Performs Demultiplexing

There is a third, independent reason why no reasonable jury could have found that the pointer processor performs the demultiplexing required by the claims, and thus there is non-infringement as a matter of law. Even if a component other than the claimed demultiplexer could perform the claimed demultiplexing, and even if the demultiplexing did not need to be completed before the error insertion, there is simply no meaningful support in the record for Dr. Prucnal's opinion that the pointer processor performs the demultiplexing required by the patent.

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[4] In *Oak Tech.*, the claim recited an error correction operation and an error detection operation for detecting errors after the error correction operation. *Id.* at 1323. The patentee argued that the claim language was "broad enough to cover a situation in which the error detection operation commences before the error correction operation is complete." *Id.* at 1324. Relying on the claim language itself, confirmed by the specification, the Federal Circuit rejected the patentee's argument, holding that the error correction operation must be "complete" before the error detection operation can occur. *Id.* at 1324-29.

Dr. Prucnal testified that a "standard" definition for a demultiplexer in the context of the '763 patent is a device that receives a multiplexed signal as its input and drops at least one demultiplexed channel at its output. D.I. 354 at 1139:5-10.

It is clear from Dr. Prucnal's testimony and the demonstratives he used at trial to illustrate how Cisco's products work that the pointer processor in Cisco's products does not satisfy even Dr. Prucnal's definition of demultiplexing. As shown in Dr. Prucnal's own demonstrative below, the signal at the output of the pointer processor is the very same red, yellow and blue multiplexed signal that the pointer processor receives as its input. It is clear from Dr. Prucnal's illustration of Cisco's products that the pointer processor does not drop any channels.

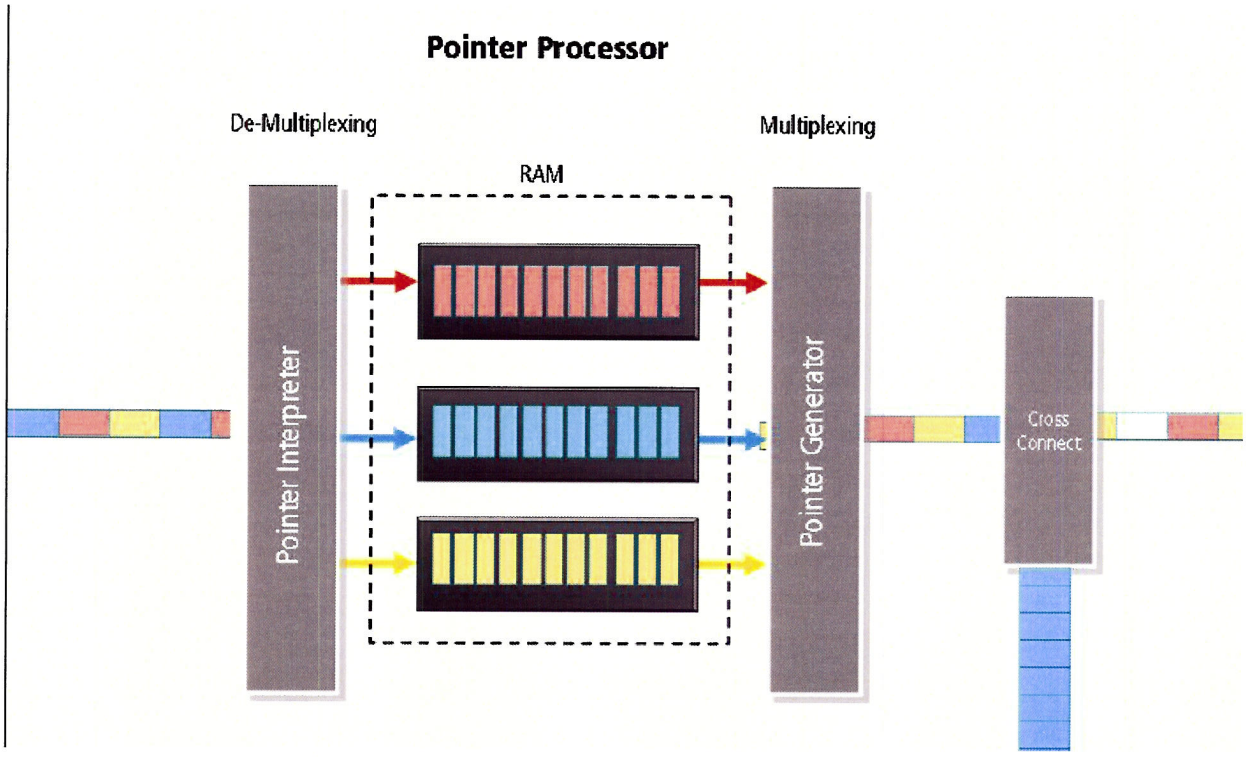

Exhibit 2 [Prucnal Demonstrative from direct examination].

Dr. Prucnal confirmed this at trial when he testified that the input to the pointer processor is a multiplexed stream and that the output is also a multiplexed stream:

> Q: The input to the pointer processor is a multiplexed stream, isn't it?
>
> A: Yes, it is.
>
> . . .
>
> Q: The output from the pointer processor, as you have depicted it, is a multiplexed stream. It is a single stream. Right?
>
> A: Generally speaking, yes. There are other stages of circuitry that I haven't included here. But ***the result I wanted to show is that after this we have a multiplexed stream.***

D.I. 354 at 1138:15 – 1139:4.

This is in sharp contrast to the cross-connect, which both experts agree is a demultiplexer. Dr. Prucnal's trial demonstrative (above) clearly shows that the cross-connect does receive a multiplexed signal as its input (shown as a combination of red, yellow and blue channels) and "drops" a demultiplexed channel from that multiplexed signal at its output (the blue channel) because that particular channel has arrived at its destination and its travel around the ring is complete. *See id.* at 1139:11-15 (Dr. Prucnal conceding that it is the cross-connect that drops channels from the multiplexed high-level signal).

In sum, because there is no dispute that the cross-connect, not the pointer processor, is the claimed demultiplexer, completes the claimed demultiplexing, and performs what Dr. Prucnal testified was the "standard" definition of demultiplexing in this context, and that all error signals are inserted before the cross-connect, no reasonable jury could have found that the error signals inserted in response to a high-level failure are inserted following demultiplexing as the Court's claim construction specifically requires.

B. No Reasonable Jury Could Have Found That The Pointer Processor Inserts Error Signals In Response To A High-Level Failure

Even if one were to assume that the pointer processor were the demultiplexer of the claims, the record establishes that Cisco's products do not infringe for an additional reason. This reason stems from the fact that the required error signals are not just any error signals, but rather must be inserted *in response to a high-level failure*. Claim 1, for example, requires the error signals to be inserted "in response to said monitoring means detecting a lack of integrity on said multiplexed communications on the first ring or the second ring or both the first ring and the second ring." PTX 7 ['763 patent] at 6:37-57. The Court construed the term "evaluating the integrity of the multiplexed subrate communications" to mean "determining whether each high-level signal is defective." D.I. 179 at 2. The claims, therefore, require error signals to be inserted in response to the monitoring means determining that a high-level signal is defective.

Dr. Grover explained that in Cisco's products, the error signals inserted by the framer (which both experts agreed is *before* the pointer processor[5]) are the error signals inserted in response to a high-level failure. D.I. 359 at 1782:1-11. Dr. Prucnal likewise admitted that it is the framer, not the pointer processor, that inserts error signals in response to a high-level failure, and that those error signals are propagated to downstream components. D.I. 354 at 1133:3-10.

Because there is no dispute that the framer inserts error signals in response to a high-level failure before, not following, the pointer processor (which Telcordia relied on at trial as performing the demultiplexing required by the claims), no reasonable jury could have found that the error signals required by the claims are inserted following demultiplexing.

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[5] It is undisputed that the framer is "upstream," *i.e.*, before, the pointer processor. D.I. 359 at 1786:16 – 1787:4; Exhibit 3 [Prucnal Demonstrative marked during cross-examination] (depicting the multiplexed signal reaching the framer (marked as number 4 during Dr. Prucnal's cross examination) before the pointer processor (marked as number 3).

Because of this undeniable technological truth, Telcordia argued that the pointer processor inserts additional error signals, on which it attempted to rely to show infringement. However, all that happens at the pointer processor is that the error signal (an all "ones" signal) that was added upstream at the framer in response to the high level failure continues to propagate through the system. While the error signal may change its format as it proceeds through the system and past the pointer processor, any reformatting of the error signal – which indisputably remains all "ones" when there is a high-level failure – is not in *response to a high level failure*; it is merely in response to the receipt of an incoming error signal.

As Dr. Grover explained, once the framer inserts an all ones error signal in response to a high-level failure, those same ones "are simply propagat[ed] down through all the subsequent block elements and components of the system." D.I. 359 at 1787:9-12; *see also id.* at 1788:19-23 ("The whole body of the signal is written as all 1's [at the framer], and then they pass through everything else downstream including the pointer processor, and they're all 1's coming in at that point and they're all 1's propagating out."). Dr. Prucnal admitted that the error signals inserted by the framer result in an all ones signal on each channel in the multiplexed high-level signal. D.I. 354 at 1134:2 – 1135:1. Dr. Prucnal also admitted that this all ones error signal simply "go[es] down into the next portion of the chip." *Id.* at 1133:3-10.

Telcordia's strained reading of the Court's claim construction is also directly contrary to the logic behind the construction. As explained above, Telcordia's infringement theory is inconsistent with the Court's construction of the asserted claims, which requires the channels to be demultiplexed before error insertion because, in contrast to Cisco's products, the system disclosed in the '763 patent is not capable of inserting error signals when the channels are multiplexed together in a high-level signal. *See* D.I. 359 at 1779:2-15 (Dr. Grover's unrebutted

testimony as to why the '763 patent requires the error signals to be inserted after demultiplexing). Because it is undisputed that the framer can and does insert error signals in response to a high-level failure before demultiplexing, it is legally irrelevant whether the same error signals are reformatted after demultiplexing.

In short, because there is no dispute that the error signals inserted in response to a high-level failure are inserted by the framer before the pointer processor and the cross-connect, no reasonable jury could have found that the error signals inserted in response to a high-level failure are inserted following demultiplexing as the Court's claim construction requires.

V. CISCO IS ENTITLED TO JUDGMENT OF INVALIDITY OF THE '763 PATENT AS A MATTER OF LAW

The asserted claims of the '763 patent are invalid because they fail to comply with the requirements of 35 U.S.C. § 112, ¶ 2. Section 112, ¶ 6 requires "means-plus-function" elements to be *clearly linked* to a structure in the specification. *See B. Braun Medical Inc. v. Abbott Labs.*, 124 F.3d 1419, 1424 (Fed. Cir. 1997). A key part of the system claimed in the '763 patent is the monitoring means that works to detect a high-level failure triggering the insertion of an error signal. During claim construction, the Court found that this means-plus-function limitation is governed by § 112, ¶ 6, and that the structure for performing this claim limitation is circuitry at a controller. However, the '763 patent does not disclose any circuitry whatsoever in connection with the "monitoring means." Nor is there any disclosure in the specification linking a controller to the claimed function of evaluating the integrity of the high-level signal. Thus, there are no structural limitations for this § 112, ¶ 6 claim element and the claims are consequently indefinite. Accordingly, as demonstrated below, the Court must find the asserted claims invalid.

A. The '763 Patent Is Invalid Under Section 112 Because There Is No Structure In The Specification Clearly Linked To The "Monitoring" Means Function

Section § 112, ¶ 2 requires patent claims to "particularly point[] out and distinctly claim[] the subject matter which the applicant regards as his invention." Claims that do not meet this requirement are invalid for indefiniteness. *In re Donaldson Co.*, 16 F.3d 1189, 1195 (Fed. Cir. 1994). "A determination of claim indefiniteness is a legal conclusion that is drawn from the court's performance of its duty as the construer of patent claims." *Default Proof Credit Card System, Inc. v. Home Depot U.S.A., Inc.*, 412 F.3d 1291, 1298 (Fed. Cir. 2005) (quoting *Atmel Corp. v. Information Storage Devices*, 198 F.3d 1374, 1378 (Fed. Cir. 1999)).

Claims written in means-plus-function format must comply with the requirements of § 112, ¶ 6, which states that a means-plus-function claim "shall be construed to cover the corresponding structure . . . described in the specification." Structure "disclosed in the specification is 'corresponding' structure only if the specification . . . *clearly links or associates* that structure to the function recited in the claim." *Braun*, 124 F.3d. at 1424. If there is no clear link between a means-plus-function element and structure described in the specification, then the patent is indefinite and invalid under § 112, ¶ 2. *Id.* at 1425; *In re Donaldson*, 16 F.3d at 1195.[6]

While this inquiry is undertaken from the point of view of one of ordinary skill in the art, "the testimony of one of ordinary skill in the art cannot supplant the total absence of structure from the specification." *Default Proof*, 412 F.3d at 1302. Using expert testimony to, in effect, "rewrite the patent's specification to create a clear link where the language in the specification

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[6] The '763 patent was issued in 1989. Prior to the decision in *Donaldson* in 1994, the United States Patent and Trademark Office ("PTO") did not apply § 112, ¶ 6 during examination. *See Donaldson*, 16 F.3d at 1194. The Federal Circuit's decision in *Donaldson* required the PTO not only to apply § 112, ¶ 6 but also to examine § 112, ¶ 6 claim terms for definiteness under § 112, ¶ 2. *Id.*

provides none" is clearly improper under controlling Federal Circuit law. *Medical Instrum. and Diagnostics Corp. v. Elekta AB*, 344 F.3d 1205, 1212 (Fed. Cir. 2003).

Here, the Court has construed the asserted claims of the '763 patent to require "*circuitry* at a controller that determines if a defect exists with the multiplexed subrate communications." It is important to appreciate that the Court has already determined that the structure of the monitoring means is *circuitry*. The remaining issue on the indefiniteness question is thus whether structures for the circuitry are disclosed in the '763 patent and clearly linked to the "monitoring means" claim element.

It is undisputedly clear from the evidence presented at trial that that the specification of the '763 patent does not disclose any structure for performing the claimed "monitoring means" functionality. Telcordia's expert Dr. Prucnal testified that the '763 patent only contains a description of "what [the monitoring means] does" and "not the circuitry itself." D.I. 354 at 1148:3-16. Likewise, Cisco's expert Dr. Grover confirmed that "the specific implementation or suggestion of circuitry at a controller for implementing that function *is simply not present*." D.I. 359 at 1816:16-18. Indeed, the words "circuit" or "circuitry" do not even appear in the specification. *Id.* at 1816:15-16.

B. Expert Testimony Cannot Cure The Absence Of Corresponding Structure

Despite the concession from its expert that the '763 patent only discloses the monitoring means function and not the required circuitry, Telcordia contended at trial that the "controller" mentioned in the patent specification is sufficient corresponding structure to preserve validity.

As a preliminary matter, the patent associates the "controller" with the functions of multiplexing signals (2:58-61), demultiplexing signals (1:29-30), and inserting error signals (4:10-12). The '763 patent does not associate the "controller" with the "monitoring means" functionality and the general reference to a controller in the patent is thus not even eligible to

serve as the corresponding structure. Thus, Telcordia's reliance on the controller fails altogether and the patent is invalid. In any event, Dr. Prucnal admitted that the controller does not disclose the circuitry structure for the monitoring means. D.I. 354 at 1147:10-16 ("controller was described . . . and for someone of ordinary skill, they would know how to interpret this and *actually build a circuit*."). Based on this testimony, counsel for Telcordia argued to the jury that "one of ordinary skill in the art with that structure would easily know how to fill the missing [piece]." D.I. 358 at 2185:1-3. It is telling that even Telcordia's counsel acknowledged that the link between the controller and the monitoring functionality is *"missing"* from the specification.

Telcordia acknowledges that the '763 patent fails to meet the fundamental structural requirement of § 112, ¶ 6, because "missing" structure cannot be "clearly linked" to a means-plus-function term. Yet Telcordia seeks to avoid the consequences of using means-plus-function claim language by substituting Dr. Prucnal's testimony for a disclosure of corresponding structure. Telcordia's argument must fail, because "the testimony of one of ordinary skill in the art cannot supplant the total absence of structure from the specification." *Default Proof*, 412 F.3d at 1302.

The Federal Circuit's decision in *Medical Instrum.* also squarely addresses and rejects Telcordia's approach. In that case, the plaintiff argued (and the district court agreed) that generic "software"[7] disclosed in the specification was corresponding structure because "techniques for performing those conversions were known to those of skill in the art at the time the application was filed." 344 F.3d at 1211. The Federal Circuit rejected this approach because it asked the

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[7] As with the "controller" in the '763 patent, in *Medical Instrum.*, the disputed "software" was corresponding structure for a variety of § 112, ¶ 6 functions related to medical imaging. The key issue addressed by the Federal Circuit was whether that software could *also* be corresponding structure for another § 112, ¶ 6 function even though the specification did not clearly link the software to the additional function.

wrong question. The right approach is to "determine whether one of ordinary skill would have understood *the specification itself to disclose the structure*, not simply whether that person would be capable of implementing that structure." *Id.* at 1212.

Telcordia's argument makes the same mistake: it focuses on whether one of ordinary skill in the art would know how to build something rather than whether the specification actually discloses and clearly links the required structure. Because the '763 patent completely fails to disclose any structures corresponding to the claimed "monitoring means," the patent is invalid.

VI. CISCO IS ENTITLED TO JUDGMENT OF INVALIDITY OF THE '633 PATENT AS A MATTER OF LAW

The following facts are undisputed. By the December 1990 CCITT Study Group XVIII meeting in Matsuyama Japan, two competing clock recovery techniques for circuit emulation had emerged as candidates for standardization: the TS (Time Stamp) and SFET (Synchronous Frequency Encoding Technique) methods. The United States representatives supported the SFET approach, developed by Bellcore (the former name of Telcordia). The French representatives backed the TS approach, developed by France Telecom. For several months, the U.S. and France pushed their respective proposals. DTX 2117 [CCITT Study Group XVIII/8 Contribution D.1123, entitled "Proposed Method to Provide the Clock Recovery Function for Circuit Emulation" (December 1990)]; DTX 2080 [CCITT Study Group XVIII Contribution D.1020, entitled "Timing Recovery for CBR Circuit Emulation," (December 1990)] (United States' Contribution comparing the TS and SFET methods and recommending SFET); DTX 2118 [CCITT Study Group XVIII Contribution D.1451, entitled "Performance Comparison of Timing Recovery Methods of CBR (June 1991)] (French Contribution comparing the TS and SFET methods and recommending TS); *see also* D.I. 353 at 576:15-577:11 (testimony of Dr. Fleischer).

By the June 1991 CCITT meeting in Geneva, the U.S. and France, and as a result the standards community, had reached an impasse. *Id.* at 576:11-23 (testimony of Dr. Fleischer); D.I. 357 at 787:12-15 (testimony of Dr. Lau); D.I. 359 at 1934:17-22 (testimony of Bellcore standards representative, Mr. Kittams); D.I. 355 at 1446:24-1448:5, 1459:11:-1460:20 (testimony of Mr. Adam).

To end this impasse, the French began working towards a potential compromise of the two competing approaches. D.I. 355 at 1447:21-1448:1 ("This bring us to have internal discussion in France Telecom in the labs to see, okay, this is our position, this is Bellcore position, how could we provide a scheme which keep each party as easy as possible, which fits the technical requirement and be acceptable for both, both parties.") (testimony of Mr. Adam).

In an August 26, 1991 facsimile, Pierre Adam of France Telecom approached Bellcore with a potential "compromise" of the competing TS and SFET methods. The first step in this proposal was acknowledging each party's objection to the other party's proposed technique:

> For the ***initialization of our discussion***, I still continue to be the interface. . . . . Our understanding of the comments on the two solutions are as follow:
>
> - for the time stamp method, ***your main objection is for the two byte overhead in the CS sublayer***;
>
> - for the SFET method, ***our main objection is in the relative higher complexity of the counters*** and the fact that a counting configuration has to match the different source bit rate to deal with. In addition, we feel that the transmission of the RSN ***can be made more robust.***

DTX 2367 [August 26, 1991 facsimile from P. Adam]. Taking the respective criticisms of the TS and SFET proposal into account, France Telecom proposed a compromise solution:

> Referring to the last sentence of "general" in annex 8 of CCITT SG XVIII/8 TD 38 page 48, ***one possible way to look for a compromise solution*** would be to consider a solution with measuring based on the TS method (but without any frame at the

> CS) and transporting the difference of frequency information carried by the reserved bit in the SAR header (***counting scheme derived from the TS method; adaptation of the SFET method to transport the clock difference information in the SAR header***). What would be your opinion on such a proposal?

Id.

Specifically, the compromise would address the France Telecom criticism of the Bellcore SFET approach by measuring the frequency difference of the clocks "based on the TS method." *Id.* However, the compromise would also address the Bellcore criticism of the TS approach (*i.e.*, "two-byte overhead in the CS sublayer") by shortening the traditional two-byte time stamp and conveying it outside the convergence sublayer overhead. *Id.* In this way, France Telecom proposed a straightforward modification of the TS approach to address both criticisms.

On September 4, 1991, Bellcore responded to France Telecom, acknowledging the France Telecom proposal and agreeing to pursue a compromise on that basis. DTX 2368 [September 4, 1991 facsimile from B. Kittams]. In a series of oral and written communications throughout the summer and fall of 1991, individuals at France Telecom and Bellcore discussed and refined this compromise proposal, which was ultimately named Synchronous Residue-Time Stamp or Synchronous Residual Time Stamp ("SRTS"). DTX 2369 [October 11, 1991 facsimile]; DTX 2370 [October 14, 1991 facsimile]; DTX 2371 [October 16, 1991 facsimile]; DTX 2372 [October 22, 1991 facsimile].

By the end of 1991, France Telecom and Bellcore presented the SRTS compromise to the standards community by having Bellcore advance it through the United States' standards body ANSI. D.I. 356 at 1491:22-1492:7 ("[w]e also receive a copy of, of the Bellcore contribution between – before it was sent to ITU, because as it was common work, Bellcore sent us the contribution for agreement.") (testimony of T. Houdoin); *id.* at 1506:25-1508:4 (testimony of J.Y. Cochennec). The stalemate having been broken, the SRTS compromise was quickly

adopted. DTX 2119 [CCITT Study Group XVIII entitled "Report of the Meeting of SWP XVIII/8-3 (Services, IVS and AAL types 1 and 2)" (December 1991)] ("D.1745 proposed ***consolidated method of both SFET and TS as the result of cooperative work darned out by USA and France.*** The method, referred to [as] SRTS (Synchronous Residual Time Stamp), combines features of both SFET and TS, thus should be considered to be the best. . . .The SWP XVIII/8-3 also expressed thanks to experts of both USA and France for their hard and patient work.").

In February of 1992, Bellcore stated in an internal patent submission that it might pursue a patent on the SRTS compromise. DTX 2684 [Patent Submission – Lab 213]. That Submission acknowledged the SRTS method as a technique "***based on*** two previously proposed methods Synchronous Frequency Encoding Technique (SFET) and Time Stamp (TS)" and that "***combines***, modifies, and improves on both SFET and TS." *Id.* Because the SRTS compromise was "submitted to CCITT SG XVIII and was accepted in Dec. 1991 as an international standard for timing recovery for constant bit rate services," the internal Bellcore document recognizes that any patent on SRTS was "likely to be patent that we will wish to ***'give away'*** in order to assure good international standard for timing recovery." *Id.*

In October 1992, Bellcore filed a patent application on the SRTS compromise. DTX 2004 ['633 patent]. The patent office issued the '978 patent – predecessor to the '633 patent – in November 1993. Bellcore did not tell France Telecom or the industry about its patent application until years later. *See, e.g.*, D.I. 356 at 1503:14-22 (testimony of J.Y. Cochennec).

A. The SRTS Compromise Was Obvious

Just one month ago – indeed during the trial in this case – the Supreme Court issued a unanimous decision in which it stressed the role of the Court as a gatekeeper in the obviousness inquiry. *KSR Intern. Co. v. Teleflex Inc.* 127 S.Ct. 1727 (2007). Acknowledging that "granting

patent protection to advances that would occur in the ordinary course without real innovation retards progress and may, in the case of patents combining previously known elements deprive prior inventions of their value entirely," the Supreme Court rejected traditional, rigid "four corners" obviousness analyses in favor a more flexible standard allowing Courts to weigh the relevant facts as appropriate in different cases. *Id.* at 1740-41. Indeed, because obviousness is ultimately a question of law, the Supreme Court underscored the role of district courts in deciding, based on a broad range of considerations, whether an invention would have been obvious to a person of ordinary skill in the art:

> ***Often, it will be necessary for a court to look to*** interrelated teachings of multiple patents; the effects of ***demands known to the design community or present in the marketplace;*** and the ***background knowledge possessed by a person having ordinary skill in the art,*** all in order to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.

KSR, 127 S.Ct. at 1740-1; *see also Leapfrog Enterprises, Inc. v. Fisher-Price, Inc.*, --- F.3d ----, 2007 U.S. App. LEXIS 10912, *9-10 (Fed. Cir. 2007) (attached as Exhibit 4) ("An obviousness determination is not the result of a rigid formula disassociated from the consideration of the facts of a case. Indeed, the ***common sense of those skilled in the art*** demonstrates why some combinations would have been obvious where others would not.") (citing *KSR*).

In applying this common-sense approach to obviousness, the Supreme Court reaffirmed the logical, but oft-overlooked, principle that consideration of the *problem* facing persons of ordinary skill in the art can be instrumental in determining whether the *solution* was obvious. Indeed, "[o]ne of the ways in which a patent's subject matter can be proved obvious is by noting that there existed at the time of invention a ***known problem for which there was an obvious solution*** encompassed by the patent's claims." *KSR*, 127 S.Ct. at 1741, 1743-46 (reversing

Federal Circuit's reversal of the district court's judgment of obviousness as a matter of law notwithstanding conflicting expert testimony).

That is precisely the situation here.

1. The SRTS Compromise Was An Obvious Solution To A Known Problem

As discussed above, by June 1991, the industry had deadlocked. Bellcore and France Telecom were each locked into their respective clock recovery techniques (SFET and TS) and had each formally articulated technical concerns with the competing proposal. Bellcore objected to the use of 16 bits of convergence sublayer overhead for timing information. France Telecom objected to the complexity and insufficient robustness of the SFET method. These conflicting positions yielded a simple problem: how to shorten the time stamp to conserve convergence sublayer overhead?

SRTS was the solution. By adopting the measurement scheme of the prior art TS approach (thus eliminating the complexity and lack-of-robustness of SFET) and modifying it to transmit timing information in fewer than 16-bits in the convergence sublayer overhead, SRTS addressed the concerns of Bellcore and France Telecom. Indeed, according to Telcordia, addressing these concerns in this way is the very essence of the claimed invention:

> Q: Now, you set forth two key aspects of the invention. One is that you use a residual time stamp that is not as large as a full time stamp and that you communicate that not in the convergent sublayer. Is one of those more important than the other?
>
> A: I wouldn't know how to judge their relative importance. I call them both important.

D.I. 357 at 924:6-15 (testimony of Telcordia's expert, Dr. Clark). In other words, the solution was: (1) a shortened time stamp (2) transmitted outside the convergence sublayer overhead.

For purposes of the obviousness inquiry, the key question is whether this solution – the SRTS compromise claimed in the '633 patent – would have been obvious to persons of ordinary skill in the art at the time. The unrebutted trial record establishes that it was.

It is undisputed that persons of ordinary skill in the art would have known of the prior art time stamp technique, exemplified in the March 1991 article authored by Julio Gonzales and Jean-Paul LeMeur of France Telecom (hereinafter, "Gonzales"). DTX 2046 [Gonzales]. Persons of ordinary skill in the art reading Gonzales and understanding the obvious drawbacks of that approach (those that Bellcore had expressed repeatedly in the standards community) would have been driven to arrive at a modified time stamp approach alleviating those problems. As set forth below, Gonzales itself would have driven persons of skill to that approach: Gonzales expressly teaches the concept of shortening the traditional time stamp to fewer than 16 bits, and a person of ordinary skill in the art reading Gonzales would, based on his or her knowledge as a skilled artisan, view transmission of the shortened time stamp outside the convergence sublayer as an obvious solution to the problem at hand. Putting two and two together, a person of ordinary skill in the art could and would easily have reached the SRTS compromise: the transmission of a shortened time stamp outside the convergence sublayer overhead.

a. Cisco Presented Overwhelming Evidence That Gonzales Teaches A Shortened Time Stamp

It is undisputed that Gonzales teaches the prior art 16-bit time stamp method. Indeed, the '633 patent itself cites Gonzales as teaching the traditional 16-bit time stamp. DTX 2004 ['633 patent] at 2:63-3:20 ("An alternative proposed approach is known as Time Stamp (TS). In the Time Stamp approach (see, for example, Gonzales et al, "Jitter Reduction in ATM Networks", Proceedings ICC '91, 9.4.1-9.4.6), the network clock is used to drive a multi-bit counter (16-bits in the proposal), which is sampled every fixed number of generated cells (e.g., 16). . . . Because

of the size of the TS (2 octets) [16 bits], it has been proposed that the TS be transmitted via the Convergence Sublayer (CS) overhead.").

Importantly, however, it is also undisputed that Gonzales expressly describes an embodiment where timing information is sent in *fewer* than 16 bits, *i.e.*, a shortened time stamp. *See* DTX 2046 [Gonzales] at 9.4.5. Although the shortened time stamp of Gonzales is not mentioned in the '633 patent's discussion of Gonzales, the disclosure in Gonzales itself describes a "2 bit" time stamp that can be used to transmit timing information so that the remaining overhead can be dedicated to other uses.[8] The testimony of Mr. Houdoin, one of the three France Telecom engineers who collaborated with Bellcore on the SRTS clock recovery technique, establishes that a person of ordinary skill in the art would read the disclosure in Gonzales to teach a shortened time stamp:

> Q: So, just to be clear, Houdoin Exhibit 2 [Gonzales] does not disclose the concept of counting the number of network clock cycles in modulo 16. Correct?
>
> A: Not modulo 16, but in the paper we don't have exact number of bits of the counter. It says that you have a certain number of bits, and, as I said before, ***for example, in Page 9.4.5 it says that only two bits are needed to represent, to represent the value of delta X, if the remaining bits – it's written in the paper.***
>
> The exact number of bits, as I have said, depends on the relative value of the reference clock and the service clock, and it's, a large part of the paper is based, deals with this

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[8] In moving for judgment as a matter of law, Telcordia's counsel suggested that the Gonzales reference cannot render the '633 patent obvious because it "doesn't teach a modulo 16 [4-bit] counter." D.I. 359 at 1999:4-6. Setting aside the fact that this question is irrelevant to the obviousness inquiry – it is, at best, relevant to anticipation by Gonzales, a theory not advanced by Cisco at trial – the record is clear that the precise length of the shortened time stamp is itself an implementation detail. D.I. 353 at 636:21-638:2 (testimony of Dr. Fleischer, including *inter alia*, "[f]our bits to my mind, I believe, although I am not a legal expert, as far as the patent is concerned, is an implementation detail.").

> fact and explains how should be the relationship between the number of bits of the time stamp, the precision of the service clock and the value of the reference clock as a relationship between these four, three variables, and it's the aim of the paper.

D.I. 356 at 1488:13-1489:4 (testimony of T. Houdoin).

Even when he continued to be pressed by Telcordia's lawyers, Mr. Houdoin confirmed that the disclosure in Gonzales would be understood by the reader as disclosing a shortened time stamp and that the precise length of that time stamp was essentially an implementation detail. *Id.* at 1493:23-1495:3 (testimony of T. Houdoin, including *inter alia*, "It's the basic idea, so you can use a counter of 16 bits or four bits or two bits or eight bits. Why not? It's the basic idea. . . . Three, four, why not? It's not a matter of which is very important. More than two bits, it was okay, so four bits, yes, four bits is a good compromise.").

Cisco's expert, Dr. Acampora, confirmed that Gonzales teaches a shortened time stamp:

> Q. Following the traditional time stamp approach, does the Gonzales article teach you anything further about achieving the SRTS compromise?
>
> A. Yes. Later on in this article, ***what Gonzales described is a technique for reducing the number of bits needed to carry this synchronization information, the timing information.***
> . . .
>
> He noted that difference, which he calls DX, in the example we gave, it would be either minus one, zero or plus one, in which case ***he concluded only two bits of information are needed to carry the timing information.***
>
> ***So if we combine that with the apparatus that he showed within the time stamp, that is strongly suggestive of the fact that, okay, we have at least reduced the number of bits needed to carry that time stamp.***

Id. at 1559:8-1560:1 (testimony of Dr. Acampora).

b. Cisco Presented Extensive Evidence That A Person Of Ordinary Skill Reading Gonzales Would Understand And Be Motivated To Transmit The Shortened Time Stamp Outside The Convergence Sublayer Overhead

Given the express disclosure of a shortened time stamp in Gonzales (the first key aspect of the claimed invention), the only open question is whether it would have been obvious to one of ordinary skill in the art at the time to transmit that shortened time stamp outside the convergence sublayer (the other key aspect of the claimed invention). Again, the record establishes that a person of ordinary skill in the art would understand and be motivated to transmit the shortened time stamp of the Gonzales reference outside the convergence sublayer. Dr. Acampora explained precisely why a person of ordinary skill in the art would be so motivated:

> A. Back up just one moment. Another aspect of the obviousness is, it's not drawn directly from this article, ***but one of skill in the art would recognize, for reasons that I mentioned earlier, if you can take the information out of the rigid confines of a layer in a protocol stack, do it. That would be obvious to anyone. So there was no reason why this time stamp information had to be carried in a convergence sublayer.***
>
> So it would be obvious that you can use, from reading this article, it is obvious you can use a shorter version of the time stamp in view of this, and ***it would be obvious to anyone skilled in the art, and don't do it in the convergence sublayer. If you can avoid locking it into a particular layer in this layered structure, if you can avoid that, avoid it.***

D.I. 356 at 1560:7-21 (testimony of Dr. Acampora); *see also id.* at 1550:5-12 ("[T]he two contributions of the SRTS technique in the invention consisted of reducing the number of bits needed to deliver the timing information, and ***taking the information out of the convergence sublayer overhead so we do not have these rigid confines. If you can do it someplace other than in a structured layer, you are much better off***.").

Indeed, the '633 patent itself explains the obvious drawback of transmitting a time stamp in the convergence sublayer, and, by extension, the benefit of moving the time stamp out of the rigid structure of that sublayer. *See* DTX 2004 ['633 patent] at 3:32-34 ("Disadvantageously however rigid convergence sublayer structure is required to transmit the TS which adds complexity and makes inefficient use of the overhead bandwidth.").

c. With Gonzales And The Knowledge Of A Skilled Artisan In Hand, A Person Of Ordinary Skill Would, Through Common Sense, Arrive At The SRTS Compromise

Combining the disclosure of Gonzales with the knowledge of a person of ordinary skill in the art, common sense dictates that a person of ordinary skill in the art would have thought to transmit a shortened time stamp outside the convergence sublayer to achieve a solution for clock recovery acceptable to both the U.S. and France in the standards process.[9] *See Leapfrog Enters.*, 2007 WL 1345333 at *4 ("Indeed, the ***common sense of those skilled in the art*** demonstrates why some combinations would have been obvious where others would not.").

2. Telcordia Failed To Rebut Cisco's Evidence Of Obviousness

In stark contrast to the evidence described above, Telcordia failed to present any testimony or evidence in rebuttal. Indeed, even with Telcordia's expert witness on the '633 patent in the courtroom, Telcordia opted to forego any rebuttal on the validity of the '633 patent and instead, chose to rely entirely on its cross-examination of Dr. Acampora. Rather than rebut

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[9] Notably, even under Dr. Fleischer's own account of how he "invented" SRTS, it took only a couple of days to come up with SRTS once he understood that there were two competing proposal for clock recovery and that the standards body was deadlocked. D.I. 353 at 577:21-578:8 (testimony of Dr. Fleischer, including *inter alia*, that "the initial insight took me no more than probably a day or two"). And, after this "initial insight" it took Dr. Fleischer only "several days" to work out some of the details and prove that SRTS would work. *Id.* at 578:8-15.

the evidence of obviousness presented in Cisco's case, however, that cross examination confirmed the already ample evidence of obviousness:

> Q. Do you believe Gonzales had everything in March 1991 to teach one of ordinary skill in the art how to make and use Claims 11 and 33? Isn't that right?
>
> A. ***If you combine Gonzales, as I testified earlier, with the knowledge of one of skill in the art that it would be desirable to take the time stamp out of the convergence sublayer, if you do that combination, then I think Gonzales does disclose the claim elements.*** If you don't do that combination, then I believe Gonzales does not disclose all the claim elements.

D.I. 356 at 1560:7-21 (cross-examination of Dr. Acampora). Indeed, Telcordia's cross-examination on Gonzales was limited to proving that Dr. Acampora did not find each element of the claims of the '633 patent expressly disclosed in Gonzales. D.I. 356 at 1690:12-1693:8. In so doing, Telcordia either failed to appreciate or wished to obfuscate the central point that Cisco was not pursuing an anticipation challenge on the basis of Gonzales.[10]

Although Telcordia may have established that Gonzales does not anticipate the claimed inventions of the '633 patent, Telcordia utterly failed to rebut the evidence that Gonzales renders those claimed inventions obvious.[11]

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[10] Indeed, in moving for judgment as a matter of law of no obviousness, Telcordia again failed to recognize the fundamental distinction between Cisco's obviousness challenge and a stalking-horse anticipation theory based on Gonzales: "[t]here is also an obviousness issue under Gonzales, which Dr. Acampora admitted ***did not anticipate*** under the Court's claim construction." D.I. 359 at 1999:2-9.

[11] Telcordia also failed to rebut the evidence Cisco presented relating to the secondary considerations of obviousness. Beyond the express teachings and suggestions of Gonzales, Dr. Acampora presented unrebutted evidence that each of the relevant secondary considerations weighed in favor of a finding of obviousness:

- No long felt need. D.I. 356 at 1562:9-16; 1562:21-1563:7 ("There was no long felt need for a revolutionary new clock recovery technique. There was an impasse in the standards body. That impasse was caused very simply by the fact of two sides were at

* * *

Here, there is no meaningful dispute as to the facts underlying Cisco's obviousness defense, only as to the ultimate legal conclusion of obviousness. Because the clear and *unrebutted* evidence of record supports, indeed compels, the legal conclusion of obviousness, Cisco requests that judgment as a matter of law be entered.

B. To The Extent There Was A Non-Obvious Invention, It Came From France Telecom

As discussed above, the record is clear that the claimed inventions of the '633 patent would have been obvious to persons of ordinary skill in the art at the time. However, even to the extent the SRTS compromise were not held obvious, the '633 patent remains invalid because the record establishes, without meaningful dispute, that whatever inventive aspects Telcordia attributes to the '633 patent, those attributes came from France Telecom. In other words, if there was an invention at all, it came from France Telecom. No reasonable jury could find otherwise.

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loggerheads. They wanted each to provide their own technique. If one side had blinked, the other one would have been immediately adapted.")

- No failure of others. *Id.* at 1563:16-20 ("There was no failure on the part of others. This was a nonproblem.")
- No commercial success or acceptance. *Id.* at 1564:3-8 ("SRTS has received little, if any, usage so I don't think there was any indication of commercial success based upon this particular technology.").
- No copying. *Id.* at 1564:13-17 ("It made its way into a standard that I don't view as being copying. That was breaking an impasse.").
- No professional recognition. *Id.* at 1564:9-12.
- No teaching away. *Id.* at 1565:5-9 ("In the Gonzales article, he pointed out there was redundancy in sending the full time stamp. He had a suggestion for removing the redundant part, most of the number of bits needed, and reducing the actual number of bits sent from 16 to two.").

1. Improper Inventorship Renders A Patent Invalid As A Matter Of Law

It is black letter law that a patent is invalid for failure to name the correct inventor or inventors. *Pannu v. Iolab*, 155 F.3d 1344, 1349-50 (Fed. Cir. 1998) ("Thus, section 102(f) still makes the naming of the correct inventor or inventors a condition of patentability; failure to name them renders a patent invalid."); *Checkpoint Sys., Inc. v. All-Tag Security S.A.*, 412 F.3d 1331, 1337-38 (Fed. Cir. 2005).

Inventorship is ultimately a question of law with underlying questions of fact. *Checkpoint Sys.*, 412 F.3d at 1338. "All that is required of a joint inventor is that he or she (1) contribute in some significant manner to the conception or reduction to practice of the invention, (2) make a contribution to the claimed invention that is not insignificant in quality, when that contribution is measured against the dimension of the full invention, and (3) do more than merely explain to the real inventors well-known concepts and/or the current state of the art." *Pannu*, 155 F.3d at 1351.

2. No Reasonable Jury Could Have Found That France Telecom Did Not Contribute The Key Aspects Of The SRTS Invention

As explained above, Telcordia's own expert contends that the claimed inventions of the '633 patent have two key aspects: (1) a shortened time stamp; and (2) transmission of that time stamp outside the convergence sublayer overhead. D.I. 357 at 924:6-15 (testimony of Telcordia's expert, Dr. Clark).

Unfortunately for Telcordia, its attempt to avoid an obviousness finding has placed it in a Catch-22: the trial record made overwhelming clear that, to the extent Telcordia is correct that these two "key aspects" are inventive, both were conceived by France Telecom and communicated by France Telecom to the named inventors at Bellcore.

a. The Record Establishes That France Telecom Conceived Of Moving The Time Stamp Out Of The Convergence Sublayer Overhead

As discussed above, the August 26, 1991 facsimile from Pierre Adam to Bellcore was the first step in breaking the impasse that had been reached in the standards community. D.I. 355 at 1447:21-1448:1, 1450:13-18, 1461:23-1462:13 (testimony of Mr. Adam). In taking that first step, France Telecom acknowledged the Bellcore objection to the traditional time stamp approach: "for the time stamp method, ***your main objection is for the two byte overhead in the CS sublayer***." DTX 2367 [August 26, 1991 facsimile from P. Adam]. To address this concern, France Telecom proposed precisely the solution that made its way into the '633 patent: moving the time stamp out of the convergence sublayer overhead so that the convergence sublayer overhead bits could be dedicated to other uses. Specifically, Mr. Adam proposed transporting a time stamp in the SAR header, *i.e.*, "without any frame at the CS":

> Referring to the last sentence of "general" in annex 8 of CCITT SG XVIII/8 TD 38 page 48, one possible way to look for a compromise solution would be to consider a solution with measuring based on the TS method ***(but without any frame at the CS)*** and transporting the difference of frequency information carried by the reserved bit ***in the SAR header*** (counting scheme derived from the TS method; ***adaptation of the SFET method to transport the clock difference information in the SAR header***). What would be your opinion on such a proposal?

DTX 2367 [August 26, 1991 facsimile from P. Adam]; *see also* D.I. 355 at 1462:2-8 (testimony of Mr. Adam); D.I. 356 at 1553:15-21 ("That is right there, without any frame at the convergen[ce] sublayer, they are clearly saying, you objected to putting this in the convergence sublayer overhead, let's take it out. Put it someplace else, so we avoid this rigidity.") (testimony of Dr. Acampora).

Importantly, named inventor Dr. Lau conceded that, prior to the August 26, 1991 facsimile from Mr. Adam, there had been no proposal to the standards community to transport

the time stamp in the SAR layer. D.I. 357 at 797:4-6 ("Q: There is no proposal before this, as you understand it, of carrying a time stamp in the SAR layer, is there? A. Correct."). Ultimately, Dr. Lau had to admit that the idea of transporting the time stamp outside the convergence sublayer overhead – which is, according to Telcordia, one of the two key aspects of the SRTS invention – came from France Telecom:

> Q. The concept of putting a time stamp in the SAR layer, meaning outside the convergen[ce] sublayer overhead, that was France Telecom's contribution, wasn't it?
>
> A. Yes.

Id. at 805:16-19; *see also* D.I. 353 at 634:21-3 (testimony of Dr. Fleischer that he "do[esn't] remember any, any discussions" as to "which sublayer it might, this information might beneficially go in.").

b. The Record Establishes That France Telecom Conceived Of The Shortened Time Stamp

The record evidence also establishes conclusively that France Telecom conceived of what Telcordia believes to be the second "key aspect" of the invention: the shortened time stamp.

In his August 26, 1991 facsimile to Bellcore, Mr. Adam proposed a compromise that addressed the other facet of Bellcore's criticism of the TS approach: that it took two bytes (16 bits) of convergence sublayer overhead. DTX 2367 [August 26, 1991 facsimile from P. Adam]; *see also* D.I. 356 at 1553:5-14 ("He is clearly suggesting we say fewer bits. One of the original Bellcore objections was two bytes. So he is clearly suggesting let's do something about that. Let's shorten – reduce the amount of information we need to deliver this timing information."); DTX 2368 [September 4, 1991 facsimile from B. Kittams] (noting that the question of exactly how long the time stamp should be was a point for further discussion).

According to Mr. Adam, the August 26 facsimile was proposing a shortened time stamp and was leaving open for future discussion exactly the length of that shortened time stamp:

> Q: And so is it, just so I understand this, or what you're saying, that at the time you wrote this letter in August of 1991 that you were leaving for another time the question of how many bits ought to be used?
>
> A: We were leaving for subsequent discussion. As long as the principle is agreed, we had to elaborate on technical, how long it was necessary, but ***basically we were confident that 16 bits were too much.***

D.I. 355 at 1456:9-16 (testimony of Mr. Adam).

Indeed, this makes sense. France Telecom was, by this point, well aware of the concept of transmitting a shortened time stamp – it had been published by France Telecom in Gonzales months before:

> Q: When you say we agree in that sentence of Houdoin Exhibit 7, you are referring to the information disclosed in exhibit 6, which is the Bellcore document dated October 11, 1991; correct?
>
> A: Not really, but, as I have said, ***we already know at this time the work from Julio Gonzales and Jean-Paul Le Muer which are written that only two bits are necessary, and that was written much earlier in 1991.*** It's document two.

D.I. 356 at 1492:14-22 (testimony of J.Y. Cochennec).

c. <u>Telcordia's Evidence Of Inventorship Is Insubstantial</u>

In contrast to the clear evidence of France Telecom's conception of the two aspects of the SRTS compromise Telcordia claims to be inventive, Telcordia's evidence of inventorship falls far short.

At trial, Telcordia's inventors presented vague, conflicting and entirely uncorroborated statements as to when and how they allegedly invented SRTS. According to Dr. Fleischer, Dr. Lau told him of the standards stalemate in late 1990 or early 1991, and after a couple of days he

had the initial insight for SRTS. D.I. 353 at 577:21-578:8, 611:12-16 (testimony of Dr. Fleischer). According to Dr. Lau's trial testimony, the concept of SRTS originated "around in the beginning of 1991 to the middle of 1991." D.I. 357 at 775:25-776:4.

However, when he was deposed, Dr. Lau had a very different answer:

> Q: Do you recall when it was that you and Mr. Fleischer conceived of the invention that's described in the '978 patent?
>
> A: Yes, roughly.
>
> Q: When was that?
>
> A: It was ***around late 1991.***

D.I. 357 at 776:14-19. When pressed on the inconsistency, Dr. Lau's only answer was "I said roughly." *Id.* at 776:21-23.

The inconsistencies in the testimony of Drs. Fleischer and Lau do not end with dates. According to Dr. Lau, he and Dr. Fleischer came up with the idea of a shortened time stamp at around the same time:

> Q. And it's your understanding, as I heard it, that you and Dr. Fleischer came up with that idea of a shortened time stamp together at about the same time?
>
> A. Yes.
>
> . . .
>
> Q. Shortened time stamp, both of you?
>
> A. Yes.

Id. at 770:24-771:6. Dr. Fleischer remembers it quite differently: "I spoke to my co-inventor, Richard Lau, and showed him, explained to him the beginning of my work. At the beginning he was actually somewhat incredulous about it, because basically it represented a large improvement." *Id.* at 578:18-22.

At trial, Telcordia presented no evidence to harmonize these differing accounts. And, unfortunately, the inconsistent and vague memories of Drs. Lau and Fleischer are not aided by corroborating written evidence.

Both Drs. Lau and Fleischer acknowledged the Bellcore policy that engineers diligently maintain dated and independently corroborated lab notebooks (to avoid just the issue we are facing here). D.I. 353 at 616:25-617:6 ("Q. And the purpose of lab notebooks as you understood it was to make certain there would be no disputes about who invented what when; is that fair? A. That is absolutely correct. Q. And there is a rigorous policy of dating personally and signing your own laboratory notebook pages; correct? A. Correct, and have it witnessed as well."); *id.* at 671:20-21. Notwithstanding this policy, Dr. Lau admitted that he was "just not diligent" and failed to keep a lab notebook. D.I. 357 at 778:2-4. Dr. Fleischer claims to have kept a lab notebook, but that the notebook is missing. D.I. 353 at 617:18-21.

Because there are no lab notebooks, the only written documentation Telcordia does have, Dr. Lau's June 6, 1991 Engineer's Notes, falls far short of corroborating or even suggesting conception of SRTS by Telcordia. PTX 519 [June 6, 1991 Engineer's Notes].[12] According to Telcordia, these notes reflect the work of Dr. Lau on a compromise clock recovery technique before the August 26 proposal from France Telecom. Unfortunately for Telcordia, however, these notes do nothing more than show that Dr. Lau was continuing work on his own preferred SFET technique in early June 1991. *See* D.I. 353 at 682:19-20 ("I was still calling it SFET at that time because there was ***no residual time stamp at that time*** and I was showing this in one

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[12] Telcordia also attempted to rely on loose-leaf handwritten notes authored by Dr. Flesicher. PTX 520 [Fleischer notes]. Initially Dr. Fleischer testified that these notes were from early in his work on SRTS. D.I. 353 at 612:23-613:9. On further cross examination however, Dr. Fleischer admitted he really had no idea when the notes were authored. *Id.* at 616:3-5.

implementation in this technique in the figure, figure 1."). Indeed, this is entirely consistent with Bellcore's formal position in the standards bodies in June 1991: that SFET should be adopted.

Accompanying the text of Dr. Lau's notes was a figure entitled "An Implementation of SFET." DTX 519 [June 6 Notes]. The figure depicts a block diagram of a circuit implementing SFET and includes a number of elements associated with the SFET method, including a one-bit counter and a "Compare and Code" box that transmits a "FEN" to a "FEN decode box." *Id.* While Telcordia's witnesses initially tried to pass this figure off as depicting SRTS, they ultimately conceded that the diagram was an implementation of SFET, just as it was entitled. D.I. 353 at 641:16-23 (testimony of Dr. Fleischer that FEN was concept from SFET); *id.* at 782:17-18 (testimony from Dr. Lau conceding that FEN is a concept from SFET not SRTS); D.I. 357 at 782:22-783:1 ("SFET used a one-bit value. Correct? A. Used a one-bit value, right. Q. SRTS does not use a one-bit value, does it? It uses four? A. Yes.") (testimony of Dr. Lau); *see also* D.I. 356 at 1573:7-11, 1574:2-4 ("This is a different way of accomplishing Bellcore's original SFET concept. This has nothing to do with SRTS.") (testimony of Dr. Acampora).

Ultimately, Dr. Fleischer had to admit on recross examination that the June 6 notes – the only document Telcordia has that predates the August 26 facsimile from France Telecom – do not reflect SRTS but instead reflect the prior art SFET technique:

> Q: So you think this ***could be SRTS?***
>
> A: I would have ***no reason to believe that***, given what I see here, and the little time I have had to look at it.
>
> Q: Well, look at it as long as you want to give the most accurate answer.
>
> A: Well, again, subject to my lack of current circuit design skill, et cetera, at this point ***it looks to me like SFET.***

D.I. 353 at 664:23-665:6. Again this makes sense: if Telcordia had a compromise solution in early June 1991, why did it not tell France Telecom?

* * *

As set forth above, the record makes overwhelmingly clear that, to the extent that the SRTS compromise eventually claimed in the '633 patent was not obvious to persons of ordinary skill in the art, France Telecom conceived of that compromise. Indeed, "because it is undisputed that the invention was conceived while Link [here, Bellcore] and Pannu [here, France Telecom] were ***engaged in a collaborative enterprise***[13] and it is furthermore undisputed that Pannu [France Telecom] ***conceived significant aspects of the invention***, Pannu [France Telecom] is ***certainly at least a co-inventor.***" *Pannu*, 155 F.3d at 1351. No reasonable jury could have found otherwise.

VII. CISCO IS ENTITLED TO JUDGMENT OF INVALIDITY OF THE '306 PATENT AS A MATTER OF LAW

At trial, Cisco proffered extensive evidence and testimony that the asserted claims of the '306 patent were anticipated by two prior art publications: (1) J.O. Limb and C. Flores, Description of FasNet – A Unidirectional Local-Area Communications Network, The Bell Systems Technical Journal, Vol. 61, No. 7 (September 1982) ("FasNet"); and (2) Z. L. Budrikis and A. N. Netravali, *A Packet/Circuit Switch*, AT&T Bell Laboratories Technical Journal, Vol. 63, No. 8 (October 1984) ("Budrikis"). *See* DTX 2053 [FasNet reference]; DTX 2056 [Budrikis reference]; D.I. 356 at 1599:20-1632:6 (testimony of Dr. Acampora explaining how each

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[13] Interestingly, the collaboration between France Telecom and Bellcore was no different in substance or form from that between Drs. Lau and Fleischer. According to Dr. Lau, the basis for their inclusion as co-inventors was their close collaboration in the form of "exchanging ideas back and forth," and making technical proposals and counterproposals. D.I. 357 at 769:17-770:12. In Dr. Lau's experience, this was the "normal process of invention." *Id.*

limitation of the asserted claims of the '306 patent is taught in FasNet and in Budrikis); Exhibit 5 [Acampora illustratives] at pp. 84-147.

Cisco offered additional evidence that, insofar as the FasNet and Budrikis references did not expressly disclose the corresponding structures required by the asserted apparatus claims, those claims were rendered obvious over a combination of FasNet and/or Budrikis and one or more of four other references, each disclosing that corresponding structure: (1) J.S. Turner, Design of an Integrated Services Packet Network, IEEE Journal on Selected Areas in Communications, Vol. SAC-4, No. 8 (November 1986) ("Turner"); (2) United States Patent No. 4,569,041, issued on February 4, 1986 to Takeuchi et al.("Takeuchi"); (3) Luderer et al., Wideband Packet Technology for Switching Systems, Innovations In Switching Technology / International Switching Symposium (March 15-20, 1987) ("Luderer"); and (4) European Patent 0 179 979 B1, issued on May 13, 1992 from European Patent Application 0 179 979 A2, published on May 7, 1986 and claiming priority to October 29, 1984 ("Baran"). *See* DTX 2061 [Turner reference]; DTX 2019 [Takeuchi patent]; DTX 2043 [Luderer reference]; DTX 2023 [Baran patent]; D.I. 356 at 1632:7-1639:16 (testimony of Dr. Acampora explaining why the asserted claims of the '633 patent are obvious in view of the combination of FasNet and/or Budrikis with Turner, Takeuchi, Luderer or Baran, and why the secondary considerations weigh in favor of obviousness); Exhibit 5 [Acampora illustratives] at pp. 147-154.

Even in the face of Cisco's comprehensive presentation, Telcordia ***chose*** not to present any rebuttal evidence on the validity of the '306 patent at all. Indeed, while it presented its '306 expert, Dr. Paul Prucnal, in its rebuttal case, Telcordia limited Dr. Prucnal's testimony to the '763 patent. Opting to rely only on cross-examination of Dr. Acampora, Telcordia again utterly failed to rebut the overwhelming evidence of invalidity presented by Cisco in its case.

It is significant that Telcordia disputed invalidity on the basis of only a single claim limitation: the limitation that "empty payload fields" be "a payload field that is empty of source data, but including bit signals of some kind, *i.e.* garbage bits." D.I. 179. Indeed, in closing, Telcordia's ***entire*** response to Cisco's validity challenge was based on the alleged lack of "garbage bits" in the FasNet and Budrikis references: "Dr. Acampora urged anticipation based on Fasnet and Budrikis, and those two suffer from the same deficiency. They don't meet his garbage bit limitation."[14] D.I. 358 at 2187:6-8 (Telcordia's closing argument).

Although Telcordia would have the jury and Court believe that Dr. Acampora admitted that the limitation is not satisfied, the record supports the exact opposite conclusion. On direct examination, Dr. Acampora explained that both the FasNet and Budrikis references disclose the garbage bits limitations because they teach frames with payload fields that are empty of source data (usable data) but must contain an indication of emptiness (garbage bits):

> Q. Did you find the next limitation, which is that the frames contain an empty payload field, met in the Fasnet reference?
>
> A. Yes.
>
> Q. Where is that?
>
> A. Whatever leaves the head end is initially unfilled, or as the Court has construed empty, it is empty of source data. There is no usable data in this slot.

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[14] Similarly, Telcordia's JMOL on '306 invalidity was limited entirely to disputing the presence of the "garbage bits" limitation in the anticipation and obviousness references. D.I. 359 at 1996:1-19 ("The first issue is on the '306 patent, there is an anticipation issue regarding two references, Budrikis and Fasnet. I think the evidence shows that there is no anticipation, that there is no system involving garbage bits as defined by the Court. . . . The next issue is obviousness of those same references Budrikis and Fasnet based on four references, as I understand them, Turner, Takeuchi, Luderer and Baran. They don't cure the problem created that I just mentioned, that is the lack of garbage bits. And Dr. Acampora, as I recall his testimony, admitted that they lack at least one claim limitation under the Court's claim instruction.").

> ***It may contain something. That something is what we refer to as being garbage bits. They don't mean anything. They are an indication of the emptiness.***
>
> In the real world, you can't send a vacuum. You can't send a frame alignment field followed by a vacuum. The transmission line, if it is a digital line, might be in the high state, corresponding to 1, or the low state, corresponding to 0, but it is never in the nothing state. It's got to be one state or the other. Whatever state it is in, it is meaningless.
>
> Those are the garbage bits. When the train starts out, it is empty. It is either in the 1 state or the 0 state. ***These are garbage bits.***

D.I. 356 at 1616:21-1617:16 (testimony of Dr. Acampora); *see also id.* at 1622:8-19; 1625:17-1626:11 (testimony of Dr. Acampora describing how Budrikis teaches the garbage bits limtiation). On cross examination, Dr. Acampora explained precisely why the inclusion of all 0s in the payload frame in the FasNet system meets this limitation. *Id.* at 1716:12-21; *see also id.* at 1720:2-19 (describing the generation of garbage bits in the Budrikis reference).[15]

In sum, the unrebutted trial record establishes conclusively that the asserted claims of the '306 patent are anticipated by the FasNet and Budrikis references, or at a minimum rendered obvious by the combination of FasNet and/or Budrikis with Turner, Takeuchi, Luderer or Baran. And critically, Telcordia's *only* argument to the contrary – that the FasNet and Budrikis

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[15] The only "evidence" in support of Telcordia's argument was its assertion that "Dr. Acampora agreed that both references transmit in a passive bus. And he also admitted that to write data on a passive bus, the payload field has to contain all zero bits and basically that limitation is not satisfied." D.I. 356 at 2187:9-13. Although Dr. Acampora acknowledged that a particular diagram in the FasNet reference involved a passive bus, there is no evidence in the record that an embodiment involving a passive bus could not meet the garbage bits limitation, nor did Dr. Acampora "basically" admit that. Moreover, Dr. Acampora made clear that other passages in the FasNet reference were not discussing that passive bus. *Id.* at 1719:9-13.

And, notably, Telcordia did not even suggest, let alone prove, that the Budrikis reference teaches the passive bus on which Telcordia apparently hinged its no invalidity argument. *Id.* at 1721:3 (Telcordia's counsel recognizing that the Budrikis diagram discussed during cross examination "definitely isn't a passive bus").

references do not teach the garbage bits limitation of the claims – is entirely unsupported by the trial record. Judgment as a matter of law is appropriate.[16]

VIII. CONCLUSION

For the reasons set forth above and on the basis of the trial record, Cisco requests that the Court enter judgment as a matter of law that (1) Cisco does not infringe the '763 patent; (2) the '763 patent is invalid for failure to meet the definiteness requirement of 35 U.S.C. § 112, ¶ 2; (3) the '633 patent is invalid as obvious, or alternatively, for improper inventorship; and (4) the '306 patent is invalid as anticipated or as obvious.

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[16] Insofar as Telcordia seeks to alter the Court's claim construction on the garbage bits limitation, or any other claim limitation, invalidity on the basis of the FasNet, Budrikis, Turner, Takeuchi, Luderer and Baran references may still be appropriate. For example, if the Federal Circuit were to alter this Court's claim construction to remove the garbage bits limitation, the asserted claims would be broader and Telcordia's sole argument of no invalidity would be mooted.

In any event, depending on the nature of any changes to the claim construction of any of the patents-in-suit on appeal, the parties would need to reconsider their invalidity and unenforceability positions, and likely would need to re-do expert discovery and summary judgment and re-try those issues. *See, e.g., Cardiac Pacemakers, Inc. v. St. Jude Med., Inc.*, 418 F. Supp. 2d 1021, 1032-1033 (D. Ind. 2006) ("St. Jude did not abandon or waive invalidity defenses that became relevant only on remand, where the court's new claim construction is broader than the original.") (quoting *Cordis Corp. v. Medtronic Ave, Inc.*, 2005 U.S. Dist. LEXIS 2260, at *8 (D. Del. Jan. 27, 2005) (attached as Exhibit 6) ("it is unrealistic to have expected Medtronic to present invalidity arguments in the original trial if it thought such arguments were futile based on the narrower claim construction at issue.")). In the event that the claim construction for any limitations of the patents-in-suit change, Cisco hereby moves for a new trial on invalidity and unenforceability, and the opportunity to provide new expert reports and request summary judgment on any new bases that arise from the revised claim constructions.

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CERTIFICATE OF SERVICE

I hereby certify that on May 31, 2007 I electronically filed the foregoing with the Clerk of the Court using CM/ECF, which will send notification of such filing to Steven J. Balick and John G. Day.

I further certify that I caused copies of the foregoing document to be served on May 31, 2007 upon the following in the manner indicated:

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